AMENDMENTS TO THE CLAIMS

Claim 1 (Original): A receiver for processing time division multiple access (TDMA) signals comprising:

a sampler for sampling a TDMA signal received from a transmission channel;

a derotator for correcting for frequency offset in the sampled TDMA signal;

a matched filter for correcting for the response of the transmission channel in the received TDMA signal;

an equalizer to which is applied an output signal from the matched filter;

a deinterleaver to deinterleave the received TDMA signal; and

a channel decoder for decoding the received TDMA signal after it is deinterleaved.

Claim 2 (Original): The receiver of claim 1 further comprising a filter for filtering the received TDMA signal before it is sampled by the sampler.

Claim 3 (Original): The receiver of claim 2 wherein the filter is an interpolation filter for upsampling the received TDMA signal.

Claim 4 (Original): The receiver of claim 2 wherein the filter is a matched filter for pulse shaping the received TDMA signal.

Claim 5 (Original): The receiver of claim 2 wherein the filter is a Nyquist filter.

Claim 6 (Original): The receiver of claim 2 wherein the filter upsamples the received TDMA signal and performs the functions of a Nyquist filter.

Claim 7 (Original): The receiver of claim 1 further comprising a scaler for adjusting the magnitude of the received TDMA signal.

Claim 8 (original): The receiver of claim 7 further comprising an automatic gain control circuit for controlling the scaler.

Claim 9 (Original): The receiver of claim 8 further comprising an estimator for determining received signal strength and providing an estimate of received signal strength to the automatic gain control circuit.

Claim 10 (Original): The receiver of claim 1 further comprising a channel impulse response estimator for estimating the response of the transmission channel and updating the coefficients of the matched filter.

Claim 11 (Original): The receiver of claim 10 further comprising a delay-epoch estimator for controlling the sampler in response to an input from the channel impulse response estimator.

Claim 12 (Original): The receiver of claim 1 further comprising a frequency offset estimator for estimating frequency offset and adjusting the derotator to response to such estimate.

Claim 13 (Original): The receiver of claim 1 further comprising a received signal quality metric indicator for measuring signal quality of the received TDMA signal.

Claim 14 (Original): The receiver of claim 13 wherein the measurement of signal quality is used to condition an output signal from the channel decoder.

Claim 15 (Original): The receiver of claim 1 further comprising a block decoder for decoding an output signal from the channel decoder.

Claim 16 (Original): A receiver for processing time division multiple access (TDMA) signals comprising:

an interpolation filter to which the TDMA signals are applied;

a pulse shaping matched filter to which is applied an output signal from the interpolation filter;

a sample selector to which is applied an output signal from the pulse shaping matched filter;

a derotator to which is applied an output signal from the sample selector;

a scaler to which is applied an output signal from the derotator;

a matched filter to which is supplied an output signal from the scaler;

an equalizer to which is applied an output signal from the matched filter;

a deinterleaver to which is applied an output signal from the equalizer;

a channel decoder to which is applied an output signal from the deinterleaver; and

a block decoder to which is applied an output signal from the channel decoder.

Claim 17 (Previously Presented): A receiver for processing time division multiple access (TDMA) signals comprising:

a sampling means for sampling a TDMA signal received from a transmission channel;

a derotating means for correcting for frequency offset in the sampled TDMA signal;

a matched filtering means for correcting for the response of the transmission channel in the received TDMA signal;

an equalizing means to which is applied an output signal from the matched filtering means;

a deinterleaving means to deinterleave the received TDMA signal; and

a channel decoding means for decoding the received TDMA signal after it is deinterleaved.

Claim 18 (Previously Presented): The receiver of claim 17 further comprising a filtering means for filtering the received TDMA signal before it is sampled by the sampling means.

Claim 19 (Previously Presented): The receiver of claim 18 wherein the filtering means is an interpolation filter for upsampling the received TDMA signal.

Claim 20 (Previously Presented): The receiver of claim 18 wherein the filtering means is a matched filter for pulse shaping the received TDMA signal.

Claim 21 (Previously Presented): The receiver of claim 18 wherein the filtering means is a Nyquist filter.

Claim 22 (Previously Presented): The receiver of claim 18 wherein the filtering means upsamples the received TDMA signal and performs the functions of a Nyquist filter.

Claim 23 (Previously Presented): The receiver of claim 17 further comprising a scaling means for adjusting the magnitude of the received TDMA signal.

Claim 24 (Previously Presented): The receiver of claim 23 further comprising an automatic gain control means for controlling the scaling means.

Claim 25 (Previously Presented): The receiver of claim 24 further comprising an estimating means for determining received signal strength and providing an estimate of received signal strength to the automatic gain control means.

Claim 26 (Previously Presented): The receiver of claim 17 further comprising a channel impulse response estimating means for estimating the response of the transmission channel and updating the coefficients of the matched filtering means.

Claim 27 (Previously Presented): The receiver of claim 26 further comprising a delay-epoch estimating means for controlling the sampling means in response to an input from the channel impulse response estimating means.

Claim 28 (Previously Presented): The receiver of claim 17 further comprising a frequency offset estimating means for estimating frequency offset and adjusting the derotating means to response to such estimate.

Claim 29 (Previously Presented): The receiver of claim 17 further comprising a received signal quality metric indicating means for measuring signal quality of the received TDMA signal.

Claim 30 (Previously Presented): The receiver of claim 29 wherein the measurement of signal quality is used to condition an output signal from the channel decoding means.

Claim 31 (Previously Presented): The receiver of claim 17 further comprising a block decoding means for decoding an output signal from the channel decoding means.

Claim 32 (Previously Presented): A receiver for processing time division multiple access (TDMA) signals comprising:

an interpolation filtering means to which the TDMA signals are applied;

a pulse shaping matched filtering means to which is applied an output signal from the interpolation filtering means;

a sample selecting means to which is applied an output signal from the pulse shaping matched filtering means;

a derotating means to which is applied an output signal from the sample selecting means;

a scaling means to which is applied an output signal from the derotating means;

a matched filtering means to which is supplied an output signal from the scaling means;

an equalizing means to which is applied an output signal from the matched filtering means;

a deinterleaving means to which is applied an output signal from the equalizing means;

a channel decoder to which is applied an output signal from the deinterleaver; and

a block decoding means to which is applied an output signal from the channel decoding means.

Claim 33 (Previously Presented): A method for processing time division multiple access (TDMA) signals comprising the steps of:

sampling a TDMA signal received from a transmission channel;

correcting for frequency offset in the sampled TDMA signal;

correcting for the response of the transmission channel in the received TDMA signal;

equalizing the response corrected TDMA signal;

deinterleaving the received TDMA signal; and

decoding the received TDMA signal after it is deinterleaved.

Claim 34 (Previously Presented): The method of claim 33 further comprising the step of filtering the received TDMA signal before it is sampled by the sampler.

Claim 35 (Previously Presented): The method of claim 34 wherein the filtering step comprises the steps of upsampling the received TDMA signal and performing the functions of a Nyquist filter.

Claim 36 (Previously Presented): The method of claim 33 further comprising the step of adjusting the magnitude of the received TDMA signal.

Claim 37 (Previously Presented): The method of claim 33 further comprising the step of measuring signal quality of the received TDMA signal.

Claim 38 (New): A wireless electronic communication device comprising:

a configurable modem processor having at least one hardware kernel plane;

a configurable channel codec processor having at least one hardware kernel plane coupled to the configurable modem processor; and

a configuration input for providing the configurable modem processor and the configurable channel codec processor with instructions and data used to configure the device to a single desired wireless communication protocol.

Claim 39 (New): The wireless electronic communication device of claim 38, wherein the instructions and data are also used to configure the configurable modem processor and the configurable channel codec processor to support a variable user number and a data rate by activating the at least two hardware kernel planes in each of the configurable modem processor and the configurable channel codec processor and deactivating any unused hardware kernel planes.

Claim 40 (New): The wireless electronic communication device of claim 38, wherein the instructions and data are also used to configure the configurable modem processor and the configurable channel codec processor to support a variable user number and a data rate by activating at least two functional blocks on the at least one hardware kernel plane in each of the configurable modem processor and the configurable channel codec processor and deactivating any unused functional blocks on at least one hardware kernel plane.

Claim 41 (New): The wireless electronic communication device of claim 38, wherein the configurable channel codec processor is coupled directly to the configurable modem processor.

Claim 42 (New): The wireless electronic communication device of claim 38, further comprising a memory coupled between the configurable channel codec processor and the configurable modem

processor, wherein the memory connects the at least one hardware kernel plane in the configurable modem processor with the at least one hardware kernel plane in the configurable codec processor according to the instructions and data from the configuration input.

Claim 43 (New): The wireless electronic communication device of claim 38, further comprising an optional configurable modem processor.

Claim 44 (New): The wireless electronic communication device of claim 38, further comprising:

a BTS card controller coupled directly to the configurable modem processor and directly to the configurable channel codec processor; and

a memory coupled via a bus to each of the configurable modem processor, the configurable channel codec processor, and the BTS card controller, wherein the memory connects the at least one hardware kernel plane in the configurable modem processor to the at least one hardware kernel plane in the configurable codec processor according to the instruction and data from the configuration input.

Claim 45 (New): The wireless electronic communication device of claim 38, further comprising:

a digital signal processor or microprocessor coupled directly to the configurable modem processor and directly to the configurable channel codec processor; and

a BTS card controller coupled to the digital signal processor or microprocessor via an internal data/control bus.

Claim 46 (New): The wireless electronic communication device of claim 38 being a base transceiver station.

Claim 47 (New): The wireless electronic communication device of claim 38 being a mobile handset.

Claim 48 (New): The wireless electronic communication device of claim 38 being a test equipment platform.

Claim 49 (New): The wireless electronic communication device of claim 38, wherein the wireless communication protocol is a TDMA protocol.

Claim 50 (New): The wireless electronic communication device of claim 38, wherein the wireless communication protocol is selected from the group consisting of IS-136, GSM, and CDMA.

Claim 51 (New): The wireless electronic communication device of claim 38, wherein the at least one of the hardware kernel planes in each of the configurable modem processor and the configurable channel codec processor is a reconfigurable collection of multiple algorithm-specific processors.

Claim 52 (New): The wireless electronic communication device of claim 51, wherein eaxh o fthe the reconfigurable collection of multiple algorithm-specific processors are interconnected by a reconfigurable interconnect.

Claim 53 (New): The wireless electronic communication device of claim 52, wherein each of the reconfigurable interconnects is selected from the group consisting of a memory, a configurable hardware circuit, and a processor.

Claim 54 (New): The wireless electronic communication device of claim 52, wherein each of the multiple algorithm-specific processors consists of a fixed portion and flexible portion.

Claim 55 (New): The wireless electronic communication device of claim 54, wherein the flexible portion of each algorithm-specific processor is configured by the instructions and data to realize functionality required by the desired wireless communication protocol.

Claim 56 (New): The wireless electronic communication device of claim 54, wherein the flexible portion of each algorithm-specific processor is activated and deactivated by the instructions and data to support a variable user number and a variable data rate.

Claim 57 (New): The wireless electronic communication device of claim 54, wherein the fixed portion of each algorithm-specific processor comprises a set of predefined functions that are used by the algorithm-specific processor.

Claim 58 (New): A wireless electronic communication device comprising:

a modem processor having at least one hardware kernel plane;

a configurable channel codec processor having at least one hardware kernel plane coupled to the configurable modem processor; and

a configuration input for providing the modem processor and the configurable channel codec processor with instructions and data used to configure the device to a single desired communication protocol.

Claim 59 (New): The wireless electronic communication device of claim 58, wherein the instructions and data are also used to configure the configurable channel codec processor to support a variable user number and a data rate by activating at least two hardware kernel planes in the channel codec processor and deactivating any unused hardware kernel planes.

Claim 60 (New): The wireless electronic communication device of claim 58, wherein the instructions and data are also used to configure the configurable channel codec processor to support a variable user number and a data rate by activating at least two functional blocks on the at least one hardware kernel plane in the configurable channel codec processor and deactivating any unused functional blocks on at least one hardware kernel plane.

Claim 61 (New): A wireless electronic communication device comprising:

a configurable modem processor having at least one hardware kernel plane;

a channel codec processor having at least one hardware kernel plane coupled to the configurable modem processor; and

a configuration input for providing the configurable modem processor and the channel codec processor with instructions and data used to configure the device to a single desired communication protocol.

Claim 62 (New): The wireless electronic communication device of claim 61, wherein the instructions and data are also used to configure the configurable modem processor to support a variable user number and a data rate by activating at least two hardware kernel planes in the configurable modem processor and deactivating any unused hardware kernel planes.

Claim 63 (New): The wireless electronic communication device of claim 61, wherein the instructions and data are also used to configure the configurable modem processor to support a variable user number and a data rate by activating at least two functional blocks on at least one hardware kernel plane in the configurable modem processor and deactivating any unused functional blocks on this hardware kernel plane.

Claim 64 (New): A wireless electronic communication device comprising:

a configurable modem processing means having at least one hardware kernel plane;

a configurable channel codec processing means having at least one hardware kernel plane coupled to the configurable modem processor; and

a configuration input means for providing the modem processor and the configurable channel codec processor with instructions and data used to configure the device to a single desired communication protocol.